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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,216	JANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,8,11-26,28,29,34-39,41,43,45,47-62 and 64-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,8,11-26,28,29,34-39,41,43,45,47-62 and 64-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 78 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 78 recites "a dielectric constant of the liquid crystal layer." Since liquid crystal layers have a high degree of dielectric constant anisotropy, it is unclear as to which crystal orientation of the liquid crystal is to be used to find this dielectric constant and compare with that of the insulating layer. For the purposes of examination, it is assumed that any organic, low dielectric constant insulating layer will meet the requirements of claim 78.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5, 11-13, 15, 19-22, 37-39, 41, 45, 47-49, 51, 55-58, 67, 68, 71, and 72 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,864,945 to Fujimori et al.

Regarding claims 1 and 37, Fujimori discloses a liquid crystal display device (figures 2-5) comprising: a first substrate (1) including a thin film transistor (9) formed thereon; a first electrode (2b) formed on the first substrate and electrically connected to the TFT (figures 2-5); a first insulating layer (3) formed on the first substrate including the TFT and the electrode (figures 2-5); the first insulating layer having a window (over 2b1 portion of electrode 2b – see figure 1), to expose predetermined region of the first electrode (2b1); a second electrode (2a) provided on the first insulating layer and electrically connected to the first electrode in the window (see figure 5; 2a extends along the sidewall of the window portion and down to contact 2b1; column 8, lines 15-20), the second electrode having an opening (electrode 2a is not present on top of portions of 2b1 – see figure 5) to expose the predetermined portion of the first electrode; a second substrate (11) including a third electrode (7) thereon (figures 1 and 3); a first gap ("db" in figure 5) between the third electrode and the first electrode; and a second gap ("da" in figure 5) between the third electrode and a surface of the second electrode, wherein the first and second gaps include a liquid crystal layer (4; see figures 2-5).

Regarding claims 2, 3, 38, and 39, Fujimori discloses that the first electrode is a transmission electrode (2b) for transmitting light supplied from an internal source (backlight), and the second electrode is a reflection electrode (2a) for reflecting light from an external source (see column 1, line 60 – column 2, line 8; column 7, lines 33-40).

Regarding claims 5 and 41, Fujimori discloses that the first gap is about twice as long as the second gap (figure 5; column 8, lines 19-38).

Regarding claim 45, Fujimori discloses that the first electrode (2b) is made of ITO (column 7, lines 15-19).

Regarding claims 11-13, 15, 47-49, and 51, Fujimori discloses that the device further includes a gate driving circuit section (column 7, lines 5-10; "gate wire" portion supplying the scan signal), where the insulating layer extends over the gate driving circuit section (see column 8, lines 10-37; the first insulating layer and reflection electrode must cover the gate wire lines, because the insulating layer and reflection electrode are only removed in the transmission window portion and not in external reflecting portions), where the first insulating layer has a dielectric constant less than that of the liquid crystal (organic resins have low dielectric constants).

Regarding claims 19-22 and 55-58, Fujimori discloses a color filter layer (5) and a thickness adjusting member (6) formed on the second substrate (figures 5 and 8), wherein the color filter layer is disposed on the thickness adjusting member (figures 5 and 8), and wherein the thickness of a first area of the color filter layer corresponding to the window (figure 5, portion over '2b1') is about twice as thick as a second area of the color filter (portion under 6 in figures 5 or 8) not corresponding to the window.

Regarding claim 67 and 71, Fujimori discloses that an end portion of the second electrode is formed on the first electrode exposed via the opening (see figure 5; electrode 2a 'ends' at the point where it contacts electrode 2b1).

Regarding claim 68 and 72, Fujimori discloses that the window (region extending from the exterior border of the sidewall of insulating layer 3 – see figure 5) is larger than the opening (region extending from the outer surface of electrode 2a formed on the sidewall of layer 3 – see figure 5).

5. Claims 75 and 77-78 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,620,655 to Ha et al

Regarding claim 75, Ha discloses a liquid crystal display device (Figures 1, 2, 7a-7f) comprising: a first substrate (111) including a first thin film transistor (132, 133, 134, etc. fig. 7b); an insulating layer (151) formed on the substrate including the first TFT (figure 7c); a first electrode (119a) formed on the insulating layer and electrically connected to the TFT (through 153; see figure 7c); a second electrode (166, 168) provided on the first electrode (figure 7e), wherein a predetermined portion of the second electrode is removed (at transmission window 155) for exposing a predetermined portion of the first electrode (figure 7F); a gate driving circuit section (149, 125, etc.) formed on the first substrate (see figures 7a-7f) a second substrate (15) including a third electrode (13) formed thereon (column 1, lines 24-36; it is apparent that the device of figure 7f is only the array substrate for the LCD, and that the color filter substrate would need to be present for the device to function as an LCD); and first and second gaps between the third electrode and the first or second electrodes, respectively, where the gaps include liquid crystal material (see figures 2 and 7F; it is apparent that the liquid crystal is disposed directly on the array substrate of figure 7F, with a color filter substrate disposed on top of the liquid crystal, as in figure 2; also see column 11, lines 50-55).

Regarding claim 77, Ha discloses that the first insulating layer covers the gate driving circuit section (see figures 7a-7f).

Regarding claim 78, Ha discloses that the first insulating layer is a low-k organic layer (claim 12, lines 48-55; BCB and acryl-based resin are low-k organic layers).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori et al. in view of U.S. Patent Publication No. 2003/0071944 to Baek.

Fujimori fails to teach that the gate driving circuit region is formed from amorphous silicon.

Baek discloses that the gate driving circuit region is formed from amorphous silicon (paragraphs 0045-0048).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate driving circuitry of Fujimori, such that the gate line structure includes amorphous silicon, as suggested by Baek. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include layers of amorphous Si in the gate line and gate driving circuitry, because doing so allows for good ohmic contacts between the metal gate lines and the semiconductor material of the TFT, while allowing for a reduction in the

number of layer deposition steps and photolithography steps (see Baek, paragraphs 0016, 0020, 0027).

8. Claims 8, 14, 17, 18, 23, 43, 50, 53, 54, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori et al. in view of U.S. Patent No. 6,295,109 to Kubo et al.

Regarding claims 8 and 43, Fujimori fails to disclose that the insulating layer is a photosensitive acryl resin having a thickness in the range of 0.5 microns-2.5 microns.

Kubo discloses that the insulating layer is a photosensitive acryl resin having a thickness of 2.5 microns (see column 49, lines 50-55; column 50, lines 10-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LCD structure of Fujimori, such that the first insulating layer is a photosensitive acryl resin having a thickness of 2.5 microns, as taught by Kubo. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a photosensitive acryl resin, because doing so allows for the reflection irregularities to be directly patterned into the insulating layer, without the need for additional photoresist deposition and removal steps, thus decreasing the cost and complexity of fabrication, as is appreciated by one skilled in the art (also see Kubo, column 49, lines 49-55). Since Kubo shows that a photosensitive acryl resin having a thickness of 2.5 microns provides the advantage of enabling direct patterning of the insulating layer while retaining properties suitable for use as an LCD insulation layer, it is well within the purview of a person skilled in the art to select such materials.

Regarding claims 14, 17, 18, 50, 53, and 54, Fujimori does not specifically disclose the structure of the TFT and the nature of how it connects with the lower (transmission) electrode.

Kubo shows a TFT structure substantially similar to that of Fujimori, wherein a gate oxide layer (54, acting as the "second insulating layer") is provided on the first substrate, and includes a contact hole (portion 'at' item 66 of figure 29a), wherein the first electrode is connected to the TFT in the contact hole (see figure 29a). Since the gate oxide layer is only removed at the transmission window, it extends into the gate driving circuit region and over gate lines 53 (also see column 55, lines 52-60),

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LCD of Fujimori by including a second insulating layer, as suggested by Kubo, such that the first electrode and TFT are connected through a contact hole in the second insulating layer, as further suggested by Kubo. The rationale is as follows: A person having ordinary skill in the art would recognize that a gate oxide layer is expected in a TFT in an LCD. Since Kubo illustrates that the gate oxide layer can be used to control the point of connection between the source/drain electrode of the TFT and the transmission electrode of the pixel, thus preventing any shorting between electrodes or the TFT active region, and since Fujimori does not show the details of the TFT structure and connection between the TFT and the pixel electrodes, a person skilled in the art would use the TFT structure taught in Kubo to provide the gate oxide layer and control the interconnections between the electrodes.

Regarding claims 23 and 59, Fujimori fails to specify the orientation of the liquid crystal layer.

Kubo teaches that the liquid crystal layer is homogeneously aligned with a tilting angle of about 0 degrees (see columns 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the liquid crystal layer of Fujimori have an orientation of zero degrees, as suggested by Kubo. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a tilting angle of 0 degrees, because Kubo shows that such an angle conveniently allows for a non-emitting display at no applied voltage, with the brightness of the display increasing with increased applied voltage, such that a grayscale display is formed (see Kubo, columns 20-23).

9. Claims 24-26, 28, 29, 34, 35, 60-62, 64, 65, 69, 70, 73, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,620,655 to Ha et al. in view of Fujimori et al.

Regarding claims 24, 60, 69, 70, 73, and 74, Ha discloses a liquid crystal display device (Figures 1, 2, 7a-7f) comprising: a first substrate (111) including a first thin film transistor (132, 133, 134, etc. fig. 7b); an insulating layer (151) formed on the substrate (figure 7c); a first electrode (119a) formed on the insulating layer and electrically connected to the TFT (through 153; see figure 7c); a second electrode (166, 168) provided on the first electrode (figure 7e), wherein a predetermined portion of the second electrode is removed (at transmission window 155) for exposing a predetermined portion of the first electrode (figure 7F); a second substrate (15) including a third electrode (13) formed thereon (column 1, lines 24-36; it is apparent that the device of figure 7f is only the array substrate for the LCD, and that the color filter substrate

would need to be present for the device to function as an LCD); and first and second gaps between the third electrode and the first or second electrodes, respectively, where the gaps include liquid crystal material (see figures 2 and 7F; it is apparent that the liquid crystal is disposed directly on the array substrate of figure 7F, with a color filter substrate disposed on top of the liquid crystal, as in figure 2; also see column 11, lines 50-55).

Ha fails to specifically disclose the structure of the second substrate comprising the color filter.

Fujimori teaches that the second substrate for an LCD advantageously comprises a color filter layer (5), the color filter having a first thickness (full thickness of layer 5) in a first area corresponding to the transmission window of the LCD and a second thickness about half of the first thickness (thickness of layer 5 under the black matrix portion 6) in a second area, corresponding to the second electrode/reflection region (see figures 5 and 8), wherein the different thicknesses are provided by a thickness adjusting member (6) that has been removed in the window portions (see figures 5, 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LCD of Ha to include the color filter/black matrix structure taught by Fujimori. The rationale is as follows: A person having ordinary skill in the art would have been motivated to obstruct the color filter layer, hence making it thinner in the reflection regions by use of a black matrix, because Fujimori shows that such a structure blocks the emission of light from areas other than the transmission window, and hence, improves the color purity and contrast of the device (see Fujimori, column 8, lines 43-50).

Regarding claims 25, 26, 61, and 62, Ha discloses that the first electrode is a transmission electrode for transmitting internally supplied light, and the second electrode is a reflection electrode for reflecting externally supplied light (see column 1, line 60 – column 2, line 12; column 10, line 65 – column 11, line 5; columns 30-45).

Regarding claims 28, 29, and 64, Ha fails to disclose the relative dimensions of the first and second gaps.

Fujimori teaches that it is preferable to have a transmission window gap be twice as large as a reflection region gap, in order to match the electrical and optical properties between the transmission and reflection modes, and hence, prevent the occurrence of image displacement or overlapping, displaced images when switching between modes (see Fujimori, column 2, lines 25-40; column 8, lines 19-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify the gap dimensions of Ha such that the first gap is twice as large as the second gap, and such that the dimensions are appropriately selected for maximum emission and contrast, as suggested by Fujimori. The rationale is as follows: A person having ordinary skill in the art would have been motivated to select a first gap that is twice as long as the second gap, because doing so improves the performance of the transflectance LCD by matching the distance through which the light travels for reflection and transmission modes, optimizes the contrast and brightness of the display, and prevents image displacement effects (see Fujimori, column 2, lines 25-40, column 8, lines 19-38). Although Ha and Fujimori fail to specifically teach a first gap of less than 3.3 microns and a second gap of less than 1.7 microns, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the

optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Regarding claim 34, Ha discloses a contact hole (153) formed in the insulating layer (figures 7c and 7d), wherein the first electrode is connected to the TFT through the contact hole (figures 7c, 7d).

Regarding claim 35, Ha discloses that the electrode surface of the contact hole is disposed at a level slightly higher than the first electrode, but lower than the second electrode, such that upon assembly of the two substrates, the second gap would be smaller than the third gap, which would be smaller than the first gap (see figures 7f and 2).

Regarding claim 65, Ha discloses a gate driving circuit (right-hand portion of substrate in figure 7f, including gate lines) on the substrate (see figure 7f).

10. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ha et al. in view of Fujimori et al. as applied to claim 24 above, and further in view of U.S. Patent No. 6,295,109 to Kubo et al.

Ha fails to specify the orientation of the liquid crystal layer.

Kubo teaches that the liquid crystal layer is homogeneously aligned with a tilting angle of about 0 degrees (see columns 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the liquid crystal layer of Ha, as modified by Fujimori, have an orientation of zero degrees, as suggested by Kubo. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a tilting angle of 0 degrees,

because Kubo shows that such an angle conveniently allows for a non-emitting display at no applied voltage, with the brightness of the display increasing with increased applied voltage, such that a grayscale display is formed (see Kubo, columns 20-23).

11. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ha et al. in view of Fujimori et al., as applied to claim 65, above, and further in view of Baek.

Ha fails to disclose that the gate driving circuit region is formed using amorphous silicon.

Baek discloses that the gate driving circuit region is formed from amorphous silicon (paragraphs 0045-0048).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate driving circuitry of Ha as modified by Fujimori, such that the gate line structure includes amorphous silicon, as suggested by Baek. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include layers of amorphous Si in the gate line and gate driving circuitry, because doing so allows for good ohmic contacts between the metal gate lines and the semiconductor material of the TFT, while allowing for a reduction in the number of layer deposition steps and photolithography steps (see Baek, paragraphs 0016, 0020, 0027).

12. Claim 76 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ha et al. in view of Baek.

Ha fails to disclose that the gate driving circuit region is formed using amorphous silicon.

Baek discloses that the gate driving circuit region is formed from amorphous silicon (paragraphs 0045-0048).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate driving circuitry of Ha, such that the gate line structure includes amorphous silicon, as suggested by Baek. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include layers of amorphous Si in the gate line and gate driving circuitry, because doing so allows for good ohmic contacts between the metal gate lines and the semiconductor material of the TFT, while allowing for a reduction in the number of layer deposition steps and photolithography steps (see Baek, paragraphs 0016, 0020, 0027).

Response to Arguments

13. Applicant's arguments filed 9/23/05 have been fully considered, and are addressed as follows:

The Applicant argues that Fujimori does not disclose a second electrode (170) electrically connected to the first electrode (150) in the window, but rather Fujimori discloses that the second electrode is connected to the first in the contact hole 3a.

The Examiner agrees that one embodiment of the invention of Fujimori, such as that depicted in figure 3, shows exactly what the Applicant asserts. A second embodiment of Fujimori, however, corresponding to figure 5 and cited in the present and previous Office Actions, clearly illustrates that the second, or reflection electrode extends down along the sidewall of the window, contacting the first electrode at the bottom corner of the window.

Additionally, column 7, lines 33-40 suggests that while the reflection film 2a does not need to cover the sidewalls of the insulating layer, it apparently may do so.

The Applicant argues that Kubo does not disclose the features of claims 1 and 37 added by amendment. The Examiner agrees, and withdraws the 35 U.S.C. 102(b) rejections using Kubo.

The Applicant argues that Ha does not disclose the features of claims 24 and 60 added by amendment, such as the structure of the color filter. The Examiner agrees, and has replaced the 102(e) rejections with 103(a) rejections using Ha and Fujimori.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

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SUPERVISORY PATENT EXAMINER
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